Amendments to the Claims

This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of Claims:

1-18. (Cancelled).

19 (Currently amended). A multiplexer circuit comprising at least two input channels and an output channel, each input channel comprising a first transmission gate which can be switched on by a select signal for connecting the input channel to the output channel, at least one of the input channels comprising a bypass circuit for preventing a current flowing through the first transmission gate from reaching the other input channel, and a second transmission gate, said multiplexer circuit further comprising a control circuit for controlling said bypass circuit,

wherein said bypass circuit is adapted to be switched on and off, ~~control circuit controls said bypass circuit dependent upon a voltage in the input channel,~~ and

~~wherein~~ said control circuit senses a voltage in the input channel and switches~~comprises a sense circuit to control~~ said bypass circuit dependent upon said ~~by sensing a~~ voltage in the input channel.

20. (Cancelled).

21. (Previously presented). The multiplexer circuit according to claim 19, wherein said control circuit comprises a sense circuit to control said bypass circuit by sensing a voltage in the input channel.

22. (Previously presented). The multiplexer circuit according to claim 19, wherein each input channel comprises a bypass circuit and a second transmission gate.

23. (Previously presented). The multiplexer circuit according to claim 22,

wherein the bypass circuit is switched on for an input channel which is not selected and is switched off for a selected input channel.

24. (Previously presented). The multiplexer circuit according to claim 19, wherein said bypass circuit comprises a pull-down circuit reducing an input voltage for the second transmission gate.

25. (Previously presented). The multiplexer circuit according to claim 19, wherein said bypass circuit is controlled by said select signal.

26. (Previously presented). The multiplexer circuit according to claim 19, wherein said bypass circuit is an NMOS transistor comprising a gate, a drain and a source, the gate of which is controlled by said select signal, the drain of which is connected with an output of said first transmission gate and the source of which is connected with ground potential.

27. (Previously presented). The multiplexer circuit according to claim 19, wherein said bypass circuit comprises a pull-up circuit increasing an input voltage for said second transmission gate.

28. (Previously presented). The multiplexer circuit according to claim 27, wherein said pull-up circuit is a PMOS transistor comprising a drain and a source, the drain of which is connected with an output of said first transmission gate and the source of which is connected with a power supply voltage level.

29. (Previously presented). The multiplexer circuit according to claim 19, wherein said control circuit controls said bypass circuit by means of said select signal and an input voltage applied to said input channel.

30. (Previously presented). The multiplexer circuit according to claim 19, wherein said bypass circuit comprises a pull-down circuit reducing an input voltage for the second transmission gate and a pull-up circuit increasing an input voltage for

said second transmission gate, wherein said control circuit controls said pull-up circuit and said pull-down circuit by means of said select signal and an input voltage applied to said input channel.

31. (Previously presented). The multiplexer circuit according to claim 30, wherein said bypass circuit comprises (a) an NMOS transistor comprising a gate, a drain and a source, the gate of which is controlled by said select signal, the drain of which is connected with an output of said first transmission gate and the source of which is connected with ground potential and (b) a PMOS transistor comprising a drain and a source, the drain of which is connected with an output of said first transmission gate and the source of which is connected with a power supply voltage level,

wherein said control circuit comprises a NAND gate the output of which is connected with the gate of said PMOS transistor and a NOR gate the output of which is connected with the gate of said NMOS transistor.

32. (Previously presented). The multiplexer circuit according to claim 31, wherein said NAND gate receives the input voltage and the inverter select signal and said NOR gate receives the input voltage and the select signal.

33. (Previously presented). The multiplexer circuit according to claim 21, wherein said sense circuit is constructed and adapted to sense a voltage in the input channel at the input of said first transmission gate or between said first transmission gate and said second transmission gate.

34. (Previously presented). A multiplexer circuit according to claim 33, wherein a pull-down bypass circuit is formed of a first NMOS transistor having a drain and a source, the drain of which is connected with an output of said first transmission gate and the source of which is connected with the ground level, and

wherein said sense circuit is formed of a PMOS transistor and a second NMOS transistor in series, the second NMOS transistor having a source and a drain, the source of the second NMOS transistor being connected to ground level and the PMOS

transistor having a source and a drain, the source being connected to an output of said first transmission gate, and

wherein the drains of said PMOS transistor and said second NMOS transistor are connected to each other and to the gate of the first NMOS transistor in the bypass circuit.

35. (Previously presented). The multiplexer circuit according to claim 33, wherein said pull up bypass circuit is formed of a first PMOS transistor having a drain and a source, the drain of which is connected with an output of said first transmission gate and the source of which is connected with power supply voltage level, and

wherein said sense circuit is formed of a second PMOS transistor and an NMOS transistor in series, the second PMOS transistor and the NMOS transistor each having a source and a drain, the source of the second PMOS transistor being connected to power supply voltage level and the source of the NMOS transistor being connected to an output of said first transmission gate, and

wherein the drains of the second PMOS transistor and the NMOS transistor are connected to each other and to the gate of the first PMOS transistor in the bypass circuit.

36. (Previously presented). An analogue-to-digital converter comprising a multiplexer circuit according to claim 19.

37. (Previously presented). A multiplexer circuit comprising at least two input channels and an output channel, each input channel comprising a first transmission gate which can be switched on by a select signal for connecting the input channel to the output channel, at least one of the input channels comprising a by-pass circuit for preventing a current flowing through the first transmission gate from reaching the other input channel, and a second transmission gate, said multiplexer circuit further comprising a control circuit for controlling said bypass circuit,

wherein said control circuit comprises a sense circuit to control said bypass circuit by sensing a voltage in the input channel, and

wherein said sense circuit is constructed and adapted to sense a voltage in the

input channel at the input of said first transmission gate or between said first transmission gate and said second transmission gate, and

wherein a pull-down bypass circuit is formed of a first NMOS transistor having a drain and a source, the drain of which is connected with an output of said first transmission gate and the source of which is connected with the ground level, and

wherein said sense circuit is formed of a PMOS transistor and a second NMOS transistor in series, the second NMOS transistor having a source and a drain, the source of the second NMOS transistor being connected to ground level and the PMOS transistor having a source and a drain, the source being connected to an output of said first transmission gate, and

wherein the drains of said PMOS transistor and said second NMOS transistor are connected to each other and to the gate of the first NMOS transistor in the bypass circuit.

38. (Previously presented). A multiplexer circuit comprising at least two input channels and an output channel, each input channel comprising a first transmission gate which can be switched on by a select signal for connecting the input channel to the output channel, at least one of the input channels comprising a by-pass circuit for preventing a current flowing through the first transmission gate from reaching the other input channel, and a second transmission gate, said multiplexer circuit further comprising a control circuit for controlling said bypass circuit,

wherein said control circuit comprises a sense circuit to control said bypass circuit by sensing a voltage in the input channel, and

wherein said sense circuit is constructed and adapted to sense a voltage in the input channel at the input of said first transmission gate or between said first transmission gate and said second transmission gate, and

wherein a pull-up bypass circuit is formed of a first PMOS transistor having a drain and a source, the drain of which is connected with an output of said first transmission gate and the source of which is connected with power supply voltage level, and

wherein said sense circuit is formed of a second PMOS transistor and an NMOS transistor in series, the second PMOS transistor and the NMOS transistor each having

a source and a drain, the source of the second PMOS transistor being connected to power supply voltage level and the source of the NMOS transistor being connected to an output of said first transmission gate, and

wherein the drains of the second PMOS transistor and the NMOS transistor are connected to each other and to the gate of the first PMOS transistor in the bypass circuit